

Xiang Ni

CONTACT INFORMATION

Siebel Center 4103
Department of Computer Science
University of Illinois at Urbana Champaign
Urbana, IL 61801 USA

Voice: (217) 418-9604
Fax: (217) 244-6306
E-mail: xiangni2@illinois.edu
WWW: charm.cs.illinois.edu/people/ni

RESEARCH INTERESTS

Parallel Computing: Performance Optimization, Fault Tolerance, Parallel Runtime Systems, Algorithms

EDUCATION

University of Illinois at Urbana Champaign, Urbana, Illinois USA

Ph.D. Candidate, Computer Science Aug 2010 - Present
Advisor: Prof. Laxmikant V. Kalé
GPA: 3.77 (includes courses for M.S.)

University of Illinois at Urbana Champaign, Urbana, Illinois USA

M.S., Computer Science Aug 2010 - May 2012

Beihang University, Beijing, China

B.E., Computer Science Sep 2006 - Jun 2010
GPA: 3.7 (overall), 3.9 (major)

WORK EXPERIENCE

Summer Intern, Lawrence Livermore National Lab May 2014 - Aug 2014

Mentor: Kathryn Mohror

Fault Tolerance: Lossy Compression for Checkpointing in HPC

Summer Intern, Walt Disney Animation Studio May 2013 - Aug 2013

Mentor: Rasmus Tamstorf

Parallel Applications: Distributed Cloth Simulation

Summer Intern, Lawrence Livermore National Lab May 2012 - Aug 2012

Mentor: Greg Bronevetsky

Performance Optimization: Autonomic Optimization of Sparse Computations

RESEARCH

PARALLEL APPLICATIONS DEVELOPMENT AND OPTIMIZATION

Scalable Cloth Simulation

- In collaboration with Disney Research, developed a distributed scalable first of its kind cloth simulation application using Charm++ parallel runtime system.
- Proposed and implemented scalable load balancing strategies and asynchronous communication optimizations suitable for irregular applications such as cloth simulation.
- Achieved 10x speedup for cloth simulation in comparison to the state-of-the-art shared memory implementation with good scaling to 384 cores.

Out-of-core Execution of HPC Applications

- Augmented the Charm++ and Adaptive MPI runtime system with support for executing applications with memory requirements larger than DRAM.

- Deployed prefetching and request aggregation to improve performance in the two-level memory system of DRAM and non-volatile memory.

PARALLEL RUNTIME TECHNIQUES FOR FAULT TOLERANCE

Handling Silent Data Corruptions in Parallel Applications

- Designed and implemented a replica based in-memory checkpointing framework to protect applications from both hard and soft errors.
- Demonstrated the scalability of the framework for Adaptive MPI and Charm++ applications using topology-aware mapping on large supercomputers.
- Currently working on compiler-based automated selective replication methods to improve the efficiency of the framework.

Reducing Checkpoint Overheads at Scale

- Developed an asynchronous checkpointing protocol to reduce the checkpointing overheads by 80% in production Charm++ and Adaptive MPI applications.
- Augmented the runtime system to overlap the checkpointing with application execution with adaptive prioritization for the application to minimize checkpointing interference.
- Ongoing work to automatically decide the optimal checkpoint strategy for various applications based on network simulation.

Alleviating Memory Pressure for Checkpointing

- Devised a method to efficiently use SSD for storing checkpoints instead of DRAM.
- Developed a framework to selectively use lossy compression techniques for storing checkpoints, and analyzed the trade-offs between the loss of precision and the compression ratio.

PUBLICATIONS

Xiang Ni, Laxmikant V. Kale, Mitigation of Failures in High Performance Computing via Runtime Techniques. SC 2015 Doctoral Showcase.

Xiang Ni, Laxmikant V. Kale, Rasmus Tamstorf, Scalable Asynchronous Contact Mechanics using Charm++. IPDPS 2015.

Esteban Meneses, **Xiang Ni**, Terry Jones, Don Maxwell, **Analyzing the Interplay of Failures and Workload on Titan Supercomputer.** CUG 2015.

Xiang Ni, Laxmikant V. Kale, Rasmus Tamstorf, Scalable Asynchronous Contact Mechanics with Charm++. SC 2014, ACM SRC poster.

Xiang Ni, Tanzima Islam, Kathryn Mohror, Adam Moody, Laxmikant V. Kale, Lossy Compression for Checkpointing: Fallible or Feasible? SC 2014, poster.

Esteban Meneses, **Xiang Ni**, Gengbin Zheng, Celso Mendes, Laxmikant V. Kale, **Using Migratable Objects to Enhance Fault Tolerance Schemes in Supercomputers.** TPDS 2014, Journal.

Bilge Acun, Abhishek Gupta, Nikhil Jain, Akhil Langer, Harshitha Menon, Eric Mikida, **Xiang Ni**, Michael Robson, Yanhua Sun, Ehsan Totoni, Lukasz Wesolowski, Laxmikant Kale. **Parallel Programming with Migratable Objects: Charm++ in Practice.** SC 2014.

Nikhil Jain, Abhinav Bhatele, **Xiang Ni**, Nicholas J. Wright, Laxmikant V. Kale. **Maximizing Network Throughput on the Dragonfly Interconnect.** SC 2014.

Xiang Ni, Esteban Meneses, Nikhil Jain, Laxmikant V. Kale. **ACR Automatic Checkpoint/Restart for Soft and Hard Error Protection**. SC 2013.

Xiang Ni, Esteban Meneses, Laxmikant V. Kale. **Hiding Checkpoint Overhead in HPC Applications with a Semi-Blocking Algorithm**. Cluster 2012.

Xiang Ni. **A Semi-Blocking Checkpoint Protocol to Minimize Checkpoint Overhead**. Master Thesis 2012.

Esteban Meneses, **Xiang Ni**, Laxmikant V. Kale. **A Message Logging Protocol for Multicore Systems**. FTXS 2012.

Gengbin Zheng, **Xiang Ni**, Laxmikant V. Kale. **A Scalable Double In-memory Checkpoint and Restart Scheme towards Exascale**. FTXS 2012.

HONORS AND
AWARDS

Selected to attend MIT EECS Rising Stars, 2015
Best Poster, LLNL Annual Student Poster Session, 2014.
Runners-up, Coding Illini Team, Intel Parallel Universe Computing Challenge, SC 2013.
National Scholarship (3/175), Beihang University, 2009.

COMPUTER SKILLS

- Programming Language: C++, C, MPI, OpenMP, Charm++, python, R
- Tools: LaTeX, gnuplot, Make, VTune